

TU



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,840	11/21/2001	Peter Irma August Barri	RAL920000112US2	3016

25299 7590 04/21/2006

IBM CORPORATION
PO BOX 12195
DEPT YXSA, BLDG 002
RESEARCH TRIANGLE PARK, NC 27709

EXAMINER

PEUGH, BRIAN R

ART UNIT	PAPER NUMBER
----------	--------------

2187

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

MAILED

APR 21 2006

Technology Center 2100

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/990,840
Filing Date: November 21, 2001
Appellant(s): BARRI ET AL.

Joscelyn G. Cockburn
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 23, 2006 appealing from the Office action mailed August 24, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Donner, "Patent Prosecution: Practice & Procedure Before the U.S. Patent Office", © 1999, The Bureau of National Affairs, Inc., p.241-247.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-4, 25, 26, 33, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Bass et al. (US# 6,460,120)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to an associated one of the **multiple (M) different buses**, which inherently facilitate data movement according to a certain bandwidth. A plurality of arbiters (**different memory controllers**) are coupled to the multiple different memories, and these different memory controllers comprise the TSM **Arbiter**. The plurality of arbiters of the TSM Arbiter control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et

al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18). The **access vector** as claimed refers to the logical address translation for data from the memory that must inherently occur due to the logical division of the memories and the associated logical simultaneous access. Although the Bass et al. reference does not specifically recite bandwidth in terms of the busses and memories, Bass et al. teaches that data can be read from the memories, which would inherently mean that the data travels at some speed relative to the bandwidth of the busses. Since Bass et al. also teaches that multiple memories may be read from simultaneously, the multiple pieces of data will be read over the multiple buses at the same time. Thus, **total bandwidth of all of the separate busses** related to the simultaneous read access is inherently **greater than the bandwidth of an individual bus** in the Bass et al. invention.

Regarding claim 2, Bass et al. teaches that the first mode may be a **read mode**, which is a sub-section of the TDM-mode in the form of read-only (col. 24, lines 59-63).

Regarding claim 3, Bass et al. teaches that the memory options may include multi-bank **DDR DRAM** (col. 9, lines 46-48).

Regarding claim 4, Bass et al. teaches partitioning the memory into at least **four banks with a buffer spread across the four banks** (col. 9, lines 55-60).

Regarding claim 25, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to an associated one of the multiple **(M) different buses**, which inherently facilitate data movement according to a certain bandwidth. A plurality of arbiters (**different memory**

controllers) are coupled to the multiple different memories, and these different memory controllers comprise the TSM **Arbiter**. The arbiters of the TSM Arbiter control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18).

Regarding claim 26, although the Bass et al. reference does not specifically recite bandwidth in terms of the busses and memories, Bass et al. teaches that data can be read from the memories, which would inherently mean that the data travels at some speed relative to the bandwidth of the busses. Since Bass et al. also teaches that multiple memories may be read from simultaneously, the multiple pieces of data will be read over the multiple buses at the same time. Thus, **total bandwidth of all of the activated separate busses** related to the simultaneous read access is inherently **greater than the bandwidth of an individual bus** in the Bass et al. invention.

Regarding claim 33, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. The DRAMs are divided (**partitioned**) into multiple **sectors** (submemories). Each of these memories is attached to an associated one of the multiple **(M) different buses**, which inherently facilitate data movement according to a certain bandwidth. Bass et al. **teaches partitioning the memory into at least four banks with a buffer spread across the four banks** (col. 9,

Art Unit: 2187

lines 55-60). A plurality of arbiters (**memory controllers**) are coupled to the multiple **different memories**, and these different memory controllers comprise the TSM **Arbiter**. The plurality of arbiters of the TSM Arbiter control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63;). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such **write control signals** for **accesses in the form of writes** or read accesses (col. 25, lines 5-31).

Regarding claim 34, The TSM Arbiter responds to a **read signal** for read accesses from any (**another**) of the **at least two of said N different memory** elements (col. 5, lines 25-31).

Claim 24 is rejected under 35 U.S.C. 103(a) as being obvious over Bartoldus et al. (US# 6,560,227) in view of Bass et al. (US# 6,460,120).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed

in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(I)(1) and § 706.02(I)(2).

Bartoldus et al., teaches a chip (controller) for **partitioning a frame into at least two parts (segments)**, where the segments are stored in N sets of 74 byte ping pong buffers (**plurality of memory elements**) (col. 2, lines 12-20). The segments are (**adjoining**) parts of the same frame, where the frame is sent over various LAN switches (**communication device**) and routing devices (col. 2, lines 1-11).

The difference between the claimed subject matter and that of Bartoldus et al., disclosed supra, is that claim 24 recites that an arbiter, in response to a request, causes data (parts) to be read simultaneously from the memory elements over separate busses.

Regarding claim 24, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to an associated one of the multiple (**M**) **different buses**, which inherently facilitate data movement according to a certain bandwidth. A plurality of arbiters (**different memory**

controllers) are coupled to the multiple different memories, and these different memory controllers comprise the TSM **Arbiter**. The arbiters of the TSM Arbiter control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Bartoldus et al. and Bass et al. before him at the time the invention was made to modify the network system of Bartoldus et al. to include the simultaneous access memories of Bass et al., because then the requested data could be retrieved from the memories in a quicker fashion and use less processing cycles.

Claim 27 is rejected under 35 U.S.C. 103(a) as being obvious over Bartoldus et al. (US# 6,560,227) in view of Bass et al. (US# 6,460,120) and Applicant's Admitted Prior Art (AAPA).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an

invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(I)(1) and § 706.02(I)(2).

Bartoldus et al., teaches a chip (controller) for **partitioning a frame into at least two parts (segments)**, where the segments are stored in N sets of 74 byte ping pong buffers (**plurality of memory elements**) (col. 2, lines 12-20). The segments are (**adjoining**) parts of the same frame, where the frame is sent over various LAN switches (**communication device**) and routing devices (col. 2, lines 1-11).

The difference between the claimed subject matter and that of Bartoldus et al., disclosed supra, is that claim 27 recites simultaneously reading data from multiple memories where the total bandwidth output from the memories matches the bandwidth of a FAT pipe port on a communication device.

Regarding claim 27, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to

an associated one of the multiple **(M) different buses**, which inherently facilitate data movement according to a certain bandwidth. A plurality of arbiters **(different memory controllers)** are coupled to the multiple different memories, and these different memory controllers comprise the TSM **Arbiter**. The arbiters of the TSM Arbiter control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18), where the read accesses are part of a read **window**. Although the Bass et al. reference does not specifically recite bandwidth in terms of the busses and memories, Bass et al. teaches that data can be read from the memories, which would inherently mean that the data travels at some speed relative to the bandwidth of the busses.

AAPA teaches that **FAT pipes** are high bandwidth channels for transmitting large amounts of data, and can be included in high-speed storage subsystems (page 2, lines 6-10).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Bartoldus et al., Bass et al., and AAPA before him at the time the invention was made to modify the network system of Bartoldus et al. to include the simultaneous access memories of Bass et al. and FAT pipe bandwidth of AAPA, because then the requested data could be retrieved from the memories in a quicker fashion and use less processing cycles according to the simultaneous access and FAT pipe features.

(10) Response to Argument

The Applicant has argued on page 7 of the response regarding the removal of U.S. Pat. No. 6,460,120 in response to the 37 CFR 1.132 Declarations as submitted.

The Applicant has argued in paragraph three of page 7 that the Declarations as submitted are proper, in light of MPEP 716.10, to remove the patent as a reference against the invention as claimed. Further, the Applicant has argued that "...the argument of the Examiner requiring further proof or showing to establish inventorship has gone far beyond and appears incongruous with the guidelines promulgated by the Patent Office and Courts".

The Examiner consulted others in regards to the sufficiency of the Declarations filed under 37 CFR 1.132, who then identified the necessary actions to be taken by the Examiner in response to the Declarations. The Examiner still maintains that the Applicant has not provided the necessary proof or showing to establish inventorship for the removal of the patent reference [see *Cooper v. Goldfarb*, 478 USPQ2d 1896; see also *Donner*, p. 241-247]. The Examiner's response to Applicant's Declarations, mailed December 8, 2004 in response to the Declarations submitted under 37 CFR 1.132 on September 20, 2004, has been included below. The Examiner contends that the Examiner's response directly applies to Applicant's arguments of page 7.

From the December 8, 2004 Office Action:

The declaration under 37 CFR 1.132 filed September 20, 2004 is insufficient to overcome the rejection of claims 1-4, 25, 26, 33, and 34 based upon a specific reference under 35 U.S.C. 102(e) as set forth in the last Office action because: the declarations fail to set forth facts and evidence supporting the submitted declarations.

Paragraph (3) of the submitted declaration recites that "To the extent that any subject matter claimed in the above-identified patent application was included in the United States Patent 6,460,120...we believe that such inclusion was based on details of the present invention disclosed by us, the inventors of the above-identified patent application."

Paragraph (4) of the submitted declaration next recites regarding that five of the inventors found in paragraph (3) of the submitted declaration that "All of those inventors frequently exchanged information within IBM, including ideas about the design of the overall system which included the invention of the above-identified patent application, as well as other inventions, including the invention claimed in the Bass et al. patent mentioned above."

The Examiner would like to point out that MPEP 715.01(c)(I) states that:

Where the applicant is one of the co-authors of a publication cited against his or her application, he or she may overcome the rejection by filing an affidavit or declaration under 37 CFR 1.131. Alternatively, the applicant may overcome the rejection by filing a specific affidavit or declaration under 37 CFR 1.132 establishing that the article is describing applicant's own work. An affidavit or declaration by applicant alone indicating that applicant is the sole inventor and that the others were merely working under his or her direction is sufficient to remove the publication as a reference under 35 U.S.C. 102(a). In re Katz, 687 F.2d 450, 215 USPQ 14 (CCPA 1982).

MPEP 715.01(c)(II) recites that:

When the unclaimed subject matter of a patent, application publication, or other publication is applicant's own invention, a rejection>, which is not a statutory bar,< on that patent or publication may be removed by submission of evidence establishing the fact that the patentee, applicant of the published application, or author derived his or her knowledge of the relevant subject matter from applicant. Moreover applicant must further show that he or she made the invention upon which the relevant disclosure in the patent, application publication, or other publication is based. In re Mathews, 408 F.2d 1393, 161 USPQ 276 (CCPA 1969); In re Facius, 408 F.2d 1396, 161 USPQ 294 (CCPA 1969).

Applicants have not shown evidence supporting, or facts alleging, that would support overcoming the rejection of the aforementioned claims under the Bass et al. reference. MPEP 715.01(c)(II) states that the "... applicant must further show that he or she made the invention upon which the relevant disclosure in the patent, application publication, or other publication is based.". Merely indicating that the application inventors "believe" that the inclusion of subject matter in the patent was based on details of the present invention disclosed by the application inventors does not constitute facts or evidence. Also, stating that the inventors "...frequently exchanged information within IBM, including ideas about the design of the overall system which included the invention of the above-identified patent application" does not constitute facts or evidence regarding the specific subject matter that applicant claims was disclosed by the applicants and included in the patent.

Further, MPEP 716.10 states that:

However, it is incumbent upon the inventors named in the application, in response to an inquiry regarding the appropriate inventorship under 35 U.S.C. 102(f) or to rebut a rejection under 35 U.S.C. 102(a) or (e), to provide a satisfactory showing by way of affidavit under 37 CFR 1.132 that the inventorship of the application is correct in that the reference discloses subject matter derived from the applicant rather than invented by the author, patentee, or applicant of the published application notwithstanding the authorship of the article or the inventorship of the patent or published application. In re Katz, 687 F.2d 450, 455, 215 USPQ 14, 18 (CCPA 1982) (inquiry is appropriate to clarify any ambiguity created by an article regarding inventorship and it is then incumbent upon the applicant to provide "a satisfactory showing that would lead to a reasonable conclusion that [applicant] is the ... inventor" of the subject matter disclosed in the article and claimed in the application).

According to MPEP 716.10, the applicant must correctly identify the inventorship of the application in regards to the subject matter in question. It is unclear to the Examiner, due to the lack of facts and evidence, as to which party truly invented the subject matter in question and which party merely included the subject matter. Because the current application and the patent do not have exactly the same inventors, and due to lack of any evidence or facts by way of an affidavit or declaration from the inventors of the aforementioned US patent, the Examiner believes that the applicant has not yet provided "a satisfactory showing that would lead to a reasonable conclusion that [applicant] is the ... inventor".

Regarding claims 1 and 2, on page 8, section B(2), para. 2-6 of response the Applicant indicated that the Bass et al. reference does not teach a single arbiter performing the functions set forth in the claims. The Applicant also argues that "...the description in Bass et al. could not be reasonably construed to teach a single arbiter having access to multiple memories...causing simultaneously reading of multiple ones...wherein total bandwidth exceeds bandwidth on single bus" (page 8, section B(2), para. 5).

As noted above by the Examiner, the single TSM arbiter of Bass et al. comprises multiple memory arbiters, and it is these multiple memory arbiters (contained within the single TSM arbiter) that perform the operations as claimed in claims 1 and 2, further discussed above in the rejection and seen in Figure 13 of the Bass et al. reference (emphasis added). The claimed subject matter does not prohibit the use of multiple sub-arbiters within a master arbiter (TSM arbiter) from performing the claimed operations.

The Examiner agrees with Applicant's argument that the Bass et al. reference does not specifically recite bandwidth in terms of busses and memories (para. 6), and that the Examiner has relied upon inherency to meet the claim limitation. However, the Applicant has indicated that "...inherency is not applicable and the admission should be construed as evidence of novelty over Bass et al.". The Examiner disagrees with the Applicant's assertion, in that the Examiner's statement of inherency has been used to illustrate the wide breadth of the claimed limitation.

Although the Bass et al. reference does not specifically recite bandwidth in terms of the busses and memories, Bass et al. teaches that data can be read from the memories, which would inherently mean that the data travels at some speed relative to the bandwidth of the busses. Since Bass et al. also teaches that multiple memories may be read from simultaneously, the multiple pieces of data will be read over the multiple buses at the same time. Thus, **total bandwidth of all of the separate busses** related to the simultaneous read access is inherently **greater than the bandwidth of an individual bus** in the Bass et al. invention (emphasis added).

The Examiner is unclear as to Applicant's assertion that the inherency is not applicable, in that the Examiner has merely pointed out how the sum of all parts (bandwidth of all buses totaled together) is greater than the bandwidth of a single bus.

Regarding claim 3, the Applicant has argued that the claim is allowable based upon dependency on claim 1 and a single arbiter for controlling the DDR DRAMs.

The Examiner has explained in reference to claims 1 and 2 that Bass et al. reference teaches the claimed subject matter, as recited and noted above. The single arbiter explanation of claims 1 and 2 also applies here to claim 3, in that Bass et al. teaches a single (TSM) arbiter for controlling DDR DRAM.

Regarding claim 4, the Applicant has argued on page 9 that the Bass et al. reference fails to teach that the memory is partitioned into at least four banks with a buffer spread across the four banks. Column 9, lines 55-60 of the Bass reference clearly recites that the memory could comprise a buffer, which is comprised within the 4 bank DDR DRAM examples as shown.

Regarding claim 25, the Applicant has argued that the Bass et al. reference does not teach a single arbiter as well as a single arbiter for simultaneously reading memories. The Applicant has argued that since the Bass et al. reference states "Each Memory Arbiter contains...", that the Bass et al. reference cannot teach a single arbiter for performing the operations as claimed. This argument is similar to that which the Applicant argued in regards to claims 1 and 2, and the Examiner's position and use of the Bass et al. reference for teaching the claimed subject matter of claim 25 coincides with the Examiner's explanation of the relevance of the Bass et al. reference for claims 1 and 2, as disclosed supra.

Regarding claim 26, the Applicant has reiterated the argument for the lack of teaching by Bass et al. for the bandwidth claim limitation as applied to claim 1. The Examiner contends that the Bass et al. reference inherently teaches the bandwidth limitations as claimed and reference above, and that the memories may be simultaneously read as also found in the Bass et al. reference in column 25, lines 6-7.

Regarding claim 33, the Applicant has reiterated the argument for the lack of teaching by Bass et al. for the single arbiter (Claim 1 limitation) as well as the buffer spread across multiple sectors of the memory (Claim 4 limitation). The Examiner's arguments for where and how the Bass et al. teaches these limitations has been included above in reference to the Examiner's response of claims 1 and 4, respectively. The Examiner has recited above in the claim rejection that the multiple sectors are

interpreted as submemories, and as recited in the previous paragraph each DDR DRAM comprises 4 banks (submemories or 'multiple sectors'). The multiple sector partitions as claimed in claim 33 can be interpreted akin to the memory partition banks of claim 1, and as disclosed in the previous paragraph a buffer comprises the four banks (the buffer is 'spread across' the 'multiple sectors', where each memory inherently requires memory sectors to store data).

Regarding claim 34, the Applicant has reiterated the argument for the lack of teaching by Bass et al. for the single arbiter (Claim 1 limitation) as well as the buffer spread across multiple sectors of the memory (Claim 4 limitation). The Examiner's arguments for where and how the Bass et al. teaches these limitations has been included above in reference to the Examiner's response of claims 1 and 4, respectively.

Regarding claim 24, which was rejected under 35 U.S.C. 103(a) over Bartoldus et al. (US# 6,560,227) in view of Bass et al. (US# 6,460,120), the Applicant has argued that the rejection is improper due to the lack of teachings for "...simultaneous reading of separate memory element, or simultaneous availability of data on separate bus or a single arbiter enabling these functions".

As previously noted by the Examiner, the Bass et al. TSM arbiter comprises multiple arbiters for performing the claimed operations, and as noted by Bass et al. the four banks of the DDRAM may be logically accessed separately and simultaneously (col. 25, lines 16-18) as allowed by the single arbiter (TSM arbiter). In reference to

Applicant's assertion for the "simultaneous" limitation, the Bass et al. reference teaches that the memories may be logically divided, and thus the reading takes place on separate (logical) memories.

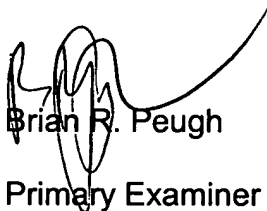
Regarding claim 27, the Applicant has indicated on page 13 that the 35 U.S.C. rejection fails to teach the claimed limitation as found in the final paragraph of the claim, beginning with "...simultaneously accessing,...". However, the Applicant has merely reciting that the references fail to teach the claim limitation and has not indicated what portion of the rejection is deficient in teaching the claimed subject matter, or argued how the references or admitted prior art does not constitute a proper 35 U.S.C. 103 rejection. Thus, the Examiner believes that the rejection attributed to claim 27 is proper.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



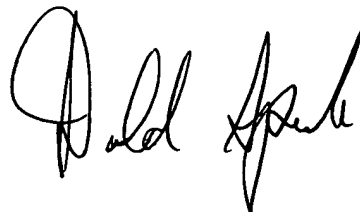
Brian R. Peugh
Primary Examiner

April 14, 2006

Conferees:

Donald Sparks

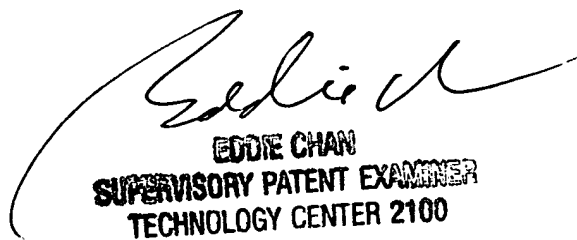
Supervisory Patent Examiner



DONALD SPARKS
SUPERVISORY PATENT EXAMINER

Eddie Chan

Supervisory Patent Examiner



EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100